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JAPANESE PATENT OFFICE

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H05K 3/46(21) Application number: **63111675**(71) Applicant: **ANDO SEIJI**(22) Date of filing: **10 . 05 . 88**(72) Inventor: **ANDO SEIJI****(54) MULTILAYER PRINTED WIRING BOARD**

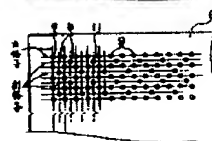
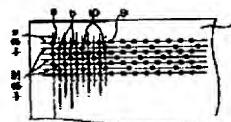
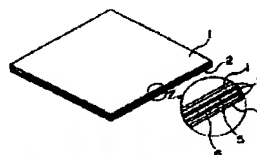
case they are seen vertically.

(57) Abstract:

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PURPOSE: To obtain a multilayer printed wiring board by forming non-conductive parts almost according among various layers at least at the main latticed intersections on the interior circuit layers while forming the other non-conductive parts in the prescribed positions on the sublatticed intersections.

CONSTITUTION: This multilayer printed wiring board has a four layer construction, wherein the first and second interior circuit layers 5 and 6 are provided between the first surface layer 1 and the second surface layer 2 through insulating layers 3. The first interior circuit layer 5 constitutes an earth pattern while the second interior circuit layer 6 constitutes a power supply pattern respectively. In the interior circuit layers 5 and 6, at least the main latticed intersection (a) is provided with the first non-conductive parts 9. Further, in the sublatticed intersections (b) provided in the different positions from the main lattice, the second and third non-conductive parts 10 and 11 are formed. These second and third non-conductive parts 10 and 11 are arranged being shifted alternately so that they may not overlap in

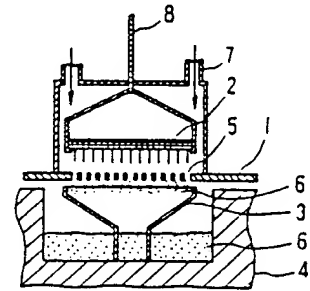


(54) PARTS EXCHANGER

(11) 1-282887 (A) (43) 14.11.1989 (19) JP
 (21) Appl. No. 63-111513 (22) 10.5.1988
 (71) HITACHI LTD (72) TAKAMORI SATO
 (51) Int. Cl. H05K3/34

PURPOSE: To reduce thermal load of a printed substrate by covering the parts with a hood and continuously performing removal of the parts whose solder is melted, and the removal of solder from the throughholes of the printed substrate.

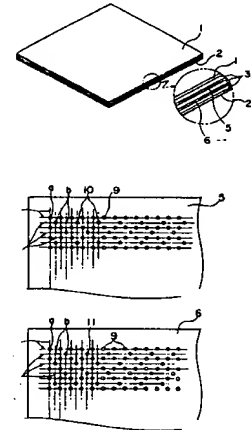
CONSTITUTION: A printed substrate 1 is set on a local soldering device 4 so that a multipinhole insertion-type LSI 2 to be removed may come above a jet nozzle 3. Next, an air blow hood 7 covers the LSI 2 to chuck the LSI 2 with a chucking mechanism 8. Next, solder 6 is made to jet upward. A local soldering device 4 heats the solder 6 in advance by a heating means locating around the recessed part, in which the solder 6 exist, for holding it in a liquid state. After the solder of the LSI 2 is heated and melted by the jet of the liquid solder 6, the chucking mechanism 8 is pulled up, the LSI 2 is removed from the printed substrate 1. Next, the solder 6 inside the throughholes 5 is blown off to the outside by air pressure.

**(54) MULTILAYER PRINTED WIRING BOARD**

(11) 1-282888 (A) (43) 14.11.1989 (19) JP
 (21) Appl. No. 63-111675 (22) 10.5.1988
 (71) SEIJI ANDO (72) SEIJI ANDO
 (51) Int. Cl. H05K3/46

PURPOSE: To obtain a multilayer printed wiring board by forming non-conductive parts almost according among various layers at least at the main latticed intersections on the interior circuit layers while forming the other non-conductive parts in the prescribed positions on the sublatticed intersections.

CONSTITUTION: This multilayer printed wiring board has a four layer construction, wherein the first and second interior circuit layers 5 and 6 are provided between the first surface layer 1 and the second surface layer 2 through insulating layers 3. The first interior circuit layer 5 constitutes an earth pattern while the second interior circuit layer 6 constitutes a power supply pattern respectively. In the interior circuit layers 5 and 6, at least the main latticed intersection (a) is provided with the first non-conductive parts 9. Further, in the sublatticed intersections (b) provided in the different positions from the main lattice, the second and third non-conductive parts 10 and 11 are formed. These second and third non-conductive parts 10 and 11 are arranged being shifted alternately so that they may not overlap in case they are seen vertically.

**(54) ELECTROMAGNETIC SHIELD OF CIRCUIT BOARD**

(11) 1-282889 (A) (43) 14.11.1989 (19) JP
 (21) Appl. No. 63-112020 (22) 9.5.1988
 (71) MATSUSHITA ELECTRIC IND CO LTD (72) KAORU SHIMIZU(2)
 (51) Int. Cl. H05K3/46, H05K9/00

PURPOSE: To plan the electrically conductive connection of an electromagnetic shield layer and a circuit pattern by performing drilling of the fixed pattern by laser in an insulating layer of a first layer on the circuit pattern and forming an electromagnetic shield layer thereon.

CONSTITUTION: In the case where a substrate 1, on which a circuit pattern 2 of copper foil, Ag-Pd and the like are arranged on the one-sided face and the inner face thereof is electrically shielded, an insulating resin layer 3 on a first layer is formed. Next earthing holes 4 of the fixed shape are drilled by laser at only necessary points in the first insulating resin layer 3 as a means for performing electric connection of an electromagnetic shield material and the circuit pattern 2. Thereafter only the fixed thickness of a conductive member layer 5 which makes an electromagnetic shield an object is formed. Further the electromagnetic shield processing of the substrate 1 is ended by lapping it on the conductive member layer 5 to form a second insulating layer 6 into the fixed thickness.

